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Implementation and Control of a Hybrid Multilevel Converter with Floating DC-links for Current Waveform Improvement

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ABSTRACT
Multilevel converters offer advantages in terms of the output waveform quality due to the increased number of levels used in the output voltage modulation. This advantage is particularly true for cascaded H-bridge converters that can be built to produce a large number of levels thanks to their modular structure. Nevertheless, this advantage comes at the cost of multiple DC-links supplied by independent rectifiers through the use of a multi-output transformer for inverters. This front- end complicates the implementation of converters that have a high number of levels. An alternative method of using lower voltage cells with floating dc-links to compensate only for voltage distortion of an NPC converter is considered for active rectifier applications. The analogy between the floating H-bridges and series active filters is used to develop a strategy for harmonic compensation of the NPC output voltage and the control of the floating dc-link voltages. This simplifies the current control scheme and increases its bandwidth. Experimental results with a low power prototype that show the good performance of the proposed modulation technique and the resulting improvement in the output waveform are provided.

***Keywords*—Power electronics, current control, harmonic distortion**

I. INTRODUCTION
In the last decade, medium-voltage high-power converters have become widely used as drives for pumps, fans and material transport in a number of industries, as well as for VAR compensation in grid applications [1], [2]. At this voltage range, multilevel converters are preferred to overcome the voltage blocking limitations of the available switches. Another important advantage of this technology is the improved output waveforms due, to the higher number of levels in the output voltage waveform, compared to the conventional three-phase two-level inverter. Similarly, an increased number of voltage levels will result in a reduced input filter size for grid connected applications. Moreover, a high number of levels allows the device switching frequency to be reduced for a given current distortion.

The multilevel topologies can be classified into three main categories: the neutral point clamped (NPC) [3], the flying capacitors (FC) [4], [5] and the cascaded H-bridge (CHB) converters [6], [7]. The three level NPC Bridge is probably the most widely used topology for medium voltage AC motor drives and PWM active rectifiers [8], [9]. NPC converters with more levels are also possible, although there are significant problems in the balancing of their dc-link capacitor voltages [10], [11], unless modified modulation strategies [12] or additionally circuitry [13] are used. On the other hand, the CHB converter is normally implemented with large number of levels, but at the cost of complicated and bulky input transformers with multiple rectifiers [7], [14], [15] or multi-winding three-phase output transformers [16]. For this reason, in applications with no active power transfer, such as in reactive power compensation, where the converter can operate without the rectifier front-end, the CHB is a highly attractive solution [17], [18].

In recent years an increased interest has been given to hybrid topologies integrating more than one topology in a single converter. Some authors have proposed the use of cascaded H-bridges fed by multilevel dc-links generated which are implemented with another converter topology [19]–[21]. In [22], a hybrid configuration based on the combination of an active NPC and a flying capacitor cell has been proposed to implement a five level converter. An hybrid converter formed by the series connection of a main three-level NPC converter and auxiliary floating H-Bridges (NPC-HBs) has been presented in [23]–[25]. In this topology, the NPC is used to supply the active power while the HBs operate as series active filters, improving the voltage waveform quality by only handling reactive power. In this way, this topology reduces the need for bulky and expensive LCL passive filters, making it an attractive alternative for large power applications [24], [25]. In this work, the control strategy for the NPC-HBs hybrid converter, previously introduced in [26], is experimentally verified. This includes: low frequency synchronous modulation of the NPC and the generation of the HBs voltage references for dc-link voltage control.

II. HYBRID TOPOLOGY
A. Power Circuit
The considered hybrid topology is composed by a traditional three-phase, three-level NPC inverter, connected with a single phase H-bridge inverter in series with each output phase [23]–[25]. The power circuit is illustrated in Fig. 1, with only the H-bridge of phase a shown in detail. For testing as an inverter, the DC source for the NPC converter is provided by two series connected diode bridge rectifiers, arranged in a twelve-pulse configuration. The H-bridge DC-links are not connected to an external DC power supply, and they consist only of floating capacitors kept at a constant voltage by the control strategy detailed in Section III.

In the hybrid topology considered, the NPC inverter pro- vides the total active power flow. For high-power medium voltage NPC, there are advantages to using latching devices such IGCTs rather than IGBTs, due to their lower losses and higher voltage blocking capability [23], [25], [27], imposing a restriction on the switching frequency. In this work, an NPC operating at a low

switching frequency (of 250Hz) is considered. In contrast, the H-bridges are rated at a lower voltage and need to be commutated at a higher frequency for an effective active filtering effect. This calls for the use of IGBT.

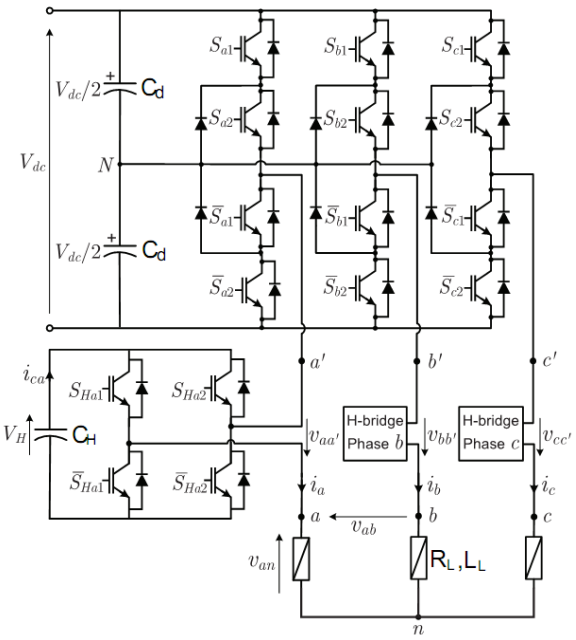

Fig. 1. Hybrid topology power circuit.

The proposed converter, shown in Fig.1, can be analyzed from two different points of view. The first interpretation is as a single hybrid multilevel inverter with a nine level phase voltage, achieved by the cascade connection of a three level NPC leg and an H-bridge per-phase. The second interpretation is as an NPC converter with a series active filter that compensates for the harmonic content introduced by the low switching NPC stage. If the NPC bridge is to be modulated at a low switching frequency, as proposed in this work, the second interpretation would seem to be more appropriate to devise a control algorithm, leading to the following two design challenges:

- To determine the lowest value of H-bridge dc-link voltage (VH) that achieves adequate voltage harmonic compensation.
- To devise a control algorithm that ensures that the floating dc-links are properly regulated at this value.

For the modulation of the NPC inverter, the Selective Harmonic Elimination (SHE) method has been selected. This method has the advantage of very low switching frequency and hence low switching losses, while eliminating the low order harmonics. With the use of SHE modulation, the fundamental output voltage of the converter is synthesized by the NPC converter and thus the series HBs will only need to supply reactive power, allowing for operation with floating capacitor DC-links.

A drawback of any synchronous modulation method, such as SHE, is its limited dynamic capability and poor closed loop performance due to the use of a pre-calculated lookup table based approach, rather than real time calculations [28]. These drawbacks can, to a large extent, be overcome by the use of the series H-bridges which are modulated in real time, introducing an additional degree of control freedom to the circuit and cleaner feedback signals.

B. NPC Selective Harmonic Elimination

Three-level SHE is an established and well documented modulation strategy [29]. A qualitative phase output voltage waveform is presented in Fig. 2 considering a 5-angle realization, so five degrees of freedom are available. This enables the amplitude of the fundamental component to be controlled and four harmonics to be eliminated. Since a three-phase system is considered, the triple harmonics are eliminated at the load by connection, and hence, they do not require elimination by the modulation pulse pattern. Thus, the 5th, 7th, 11th and 13th harmonics are chosen for elimination. For line-connected applications, this 5-angle implementation results in a switching frequency of 250Hz for the NPC portion of the converter and leaves the 17th as the first harmonic component to appear in the steady state load current. On the other hand, for variable frequency drive applications, the number of angles must be varied in order to maintain a near constant switching frequency at any operation point [30].

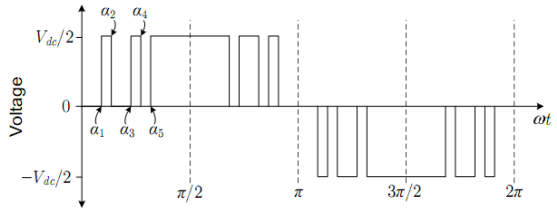

Fig. 2. Three-level NPC selective harmonic elimination phase voltage (v_{aN}) waveform.

C. H-Bridge floating DC-link voltage determination

The addition of the series H-bridge results in more levels being added on the output voltage waveform of the converter v_{aN} . In particular, if the value of V_H is smaller than V_{dc} /4, no redundant switching states are created and the output voltage waveform of the converter will have the maximum number of levels (nine), generating similar waveforms to those achieved by cascade H-bridge inverters with unequal dc sources [1], [31].

The increased number of output levels leads to a reduction in both the ΔV of the output voltage waveform and the harmonic content of the overall output voltage vaN , enhancing the power quality of the hybrid converter. One logical solution would be to make VH equal to a sixth of the NPC total dc-link voltage, i.e. VH = Vdc /6, so that equally spaced output voltage levels would be created. On the other hand, considering that the NPC converter is modulated using the synchronous SHE method, the H-bridge should be modulated to compensate for the distortion created by the modulation of the NPC. This is done at a higher frequency using carrier based unipolar PWM. When deciding the value for the dc-link voltage of the H- bridges VH , a sufficiently large value should be selected to achieve appropriate compensation of the remaining distortion, while at the same time the value of VH should be kept as low as possible in order to minimize the additional switching losses.

The voltage distortion remaining from the SHE modulation of the NPC converter can be computed as the

difference from the NPC output voltage and the reference value. The NPC output voltage is calculated including the interaction between the phases, i.e. excluding the common mode voltage from the resulting waveform. In Fig. 3a, the NPC SHE output pattern and the corresponding reference are shown. The load phase voltage resulting from the interaction of the three phases through the load neutral, as shown in Fig. 3b, is used to compute the H-bridge reference as the difference between this signal and the reference. This results in a reference signal with lower amplitude than that calculated directly from the SHE patterns, as shown in Fig. 3c. The peak value of this harmonic reference voltage varies, depending on the modulation index as illustrated in Fig. 4 for the best and worst case, respectively. On the other hand, Fig. 4b) suggests that, if VH was limited to a lower value, e.g. 0.167·Vdc , over modulation would occur but only for short periods since the peaks in the harmonic voltage reference waveform have a low voltage-time area. In other words, a compromise between the value of VH and the error incurred by over-modulating the HBs has to be found. A methodology for the solution of this tradeoff is described in [26] and from this, it can be concluded that the best compensation is obtained for values of VH between 0.167·Vdc and 0.25·Vdc . Owing to the compromise between compensation and minimization of the switching losses in the H-bridges, a value of 0.167·Vdc is used for VH in this work. To estimate the H-bridge switching losses the following considerations are made:

- The blocking voltage of their semiconductors is one third of the blocking voltage of the NPC switches, and hence, lower nominal voltage devices can be used.
- The lower the nominal blocking voltage of a semiconductor, the faster the switching and the lower the switching losses.
- The current in both converters is the same.

For switches with approximately 1:3 nominal voltage ratio and with similar current rating (e.g. 1.7kV, 1200A IGBT and 4.5kV IGCT, 1100A [32], [33] respectively), the ratio between the switching energy losses is around 1:8 . Then, considering the number of commutations in an H-bridge and in one NPC leg, the losses ratio as a function of their average switching frequencies can be expressed as:

$$\frac{P_h}{P_{npc}} = \frac{f_h}{8 f_{npc}} \qquad (1)$$

Hence, as the synchronous pulse pattern results in an average switching frequency of 250Hz for the NPC, the H-bridge PWM carrier frequency is set to 2kHz.

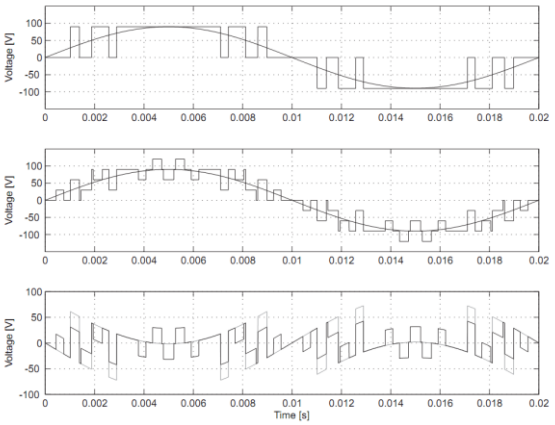

Fig. 3. H-bridge reference voltage generation for $m = 0.8$: a) NPC SHE pattern, b) load phase voltage, c) H-bridge harmonic reference with black) and without (gray) common mode voltage.

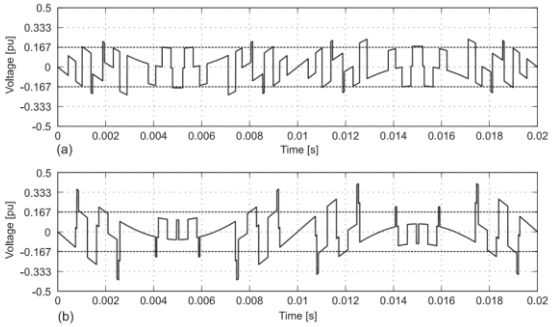

Fig. 4. H-bridge reference voltage and carrier waveform, in pu respect to V_{dc}: a) for $m = 0.8$, b) for $m = 0.89$.

III. CONTROL STRATEGY

A. H-bridge controller

Each series H-bridge converter is independently controlled by two complementary references, as shown in Fig. 5. The first

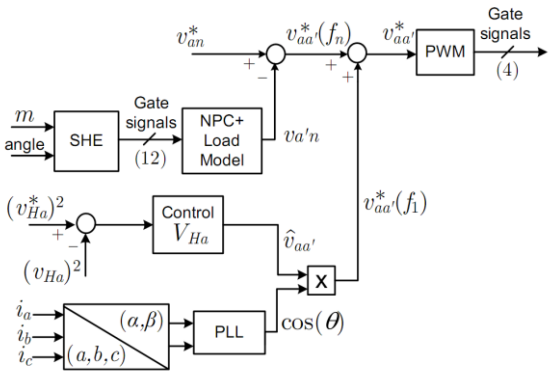

Fig. 5. H-bridge control diagram for phase *a*.

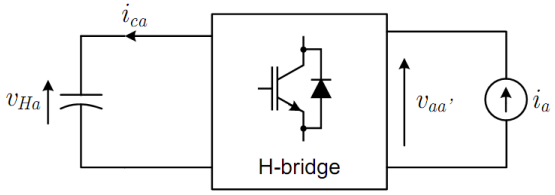

Fig. 6. Simplified H-bridge circuit for dynamic modeling of dc-link voltage

Reference V*aa'(fn) corresponds to the inverse of the harmonics remaining from the SHE pulse pattern, calculated as described in the previous section from the

difference between the NPC pulsed voltage pattern and its sinusoidal voltage reference. This calculation provides a fast and straightforward distortion estimation allowing for simple feed-forward compensation. Moreover, this voltage does not have a fundamental voltage component and hence it does not affect the floating average DC-link capacitor voltage. Nevertheless, to achieve start-up capacitor charge and to compensate voltage drift due to transient operation, an additional reference component for DC- link voltage control is included. This second component of the voltage reference V*aa'(fn) corresponds to a signal in phase with the load current. This voltage is used to inject small amounts of active power into the cell in order to control the H-bridge DC-link voltage at its reference value VH*.

During operation, the fundamental load current is generated by the NPC converter. In order to synchronize the voltage reference V*aa'(fn) with this current, a phase lock loop (PLL) algorithm is used, which guarantees zero phase shift between both signals and therefore maximizes the active power transfer to the capacitors for any power factor. The magnitude of this voltage reference is obtained from the DC-link voltage controller shown in Fig. 5. For the design of this voltage controller, the dynamic model (2) of the dc-link voltage vH a as a function of vˆaa/ is used. This model has been developed based on an instantaneous active power balance applied to the simplified cell circuit of Fig. 6.

$$\frac{C_H}{2} \cdot \frac{dv_{Ha}^2}{dt} \approx \frac{\hat{i}_a \cdot \hat{v}_{aa'}}{2}. \quad (2)$$

A undesirable characteristic of (2) is its nonlinearity with respect to vH a . This can be dealt with by linearization or by simply introducing the auxiliary variable x = v2 Ha and controlling x directly. As is indicated in Fig. 5, the latter alternative is implemented in this work. Finally, the transfer function can be expressed as (3), which is first order and can reference vH2 ∗

$$\frac{X(s)}{\hat{V}_{a'a}(s)} \approx \frac{\hat{i}_a}{C_H \cdot s} \quad (3)$$

B. External current control loop

For good dynamic performance, an outer load current loop can be implemented as shown in Fig. 7. As low order har monics are compensated by the H-bridges, the current can be synchronously sampled with the H-bridge carrier, providing a good estimation of its fundamental value. Moreover, as a high sampling frequency is used, a high current bandwidth can be achieved.

It is important to note that, in applications with low frequency switching patterns, such as the SHE modulation, the use of direct synchronous sampling of the currents is not adequate to obtain the fundamental current because the switch ing harmonics do not cross zero at regular intervals. Instead observers are needed to extract the fundamental current values [34] otherwise complex nonlinear control schemes are required [35]. In the present work, this problem is overcome by the compensating effect of the series connected H-bridges, which moves the spectra from the non-eliminated SHE harmonics to the high frequency H-bridge carrier band. This effectively simplifies the outer load current control loop design, resulting in a standard dq frame linear current regulator as shown in Fig. 7.

C. H-bride DC-link voltage control under regenerative operation

In regenerative operation, such as active front end applications for regenerative drives, the power flow needs to be controlled bidirectionally. This is possible due to the interaction between the converter and load voltages through the grid impedance, usually an inductive filter. As indicated in Fig. 8, under the regenerative operation, the load current flow is inverted. Under these conditions, the PLL of Fig. 5 will detect the absolute current phase. This means that a positive reference for the fundamental voltage amplitude vˆaa/ > 0 still implies a positive power flow into the cell and hence an increase in the DC-link voltage level vH a . Likewise, a negative fundamental voltage amplitude vˆaa/ < 0 produces a reduction in the DC-link voltage level. In other words, the control for the H-bridge cell is effective, irrespective of the direction of power flow. Therefore the technique can be applied without modification for inverter or rectifier mode of operation.

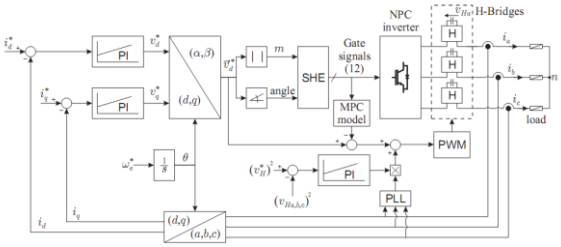

Fig. 7. Simplified current control loop for the proposed topology, including SHE for the NPC (the control loops for the H-bridges are not shown).

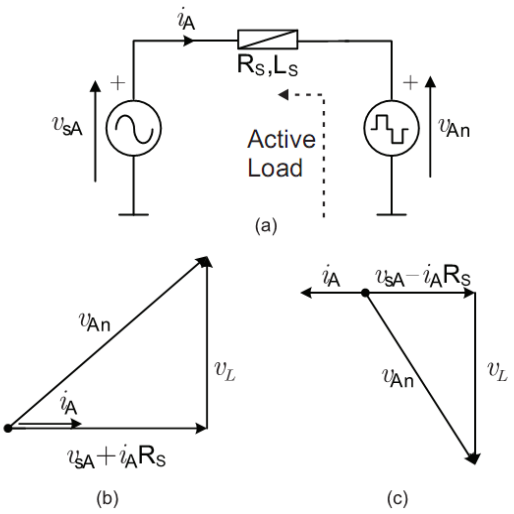

Fig. 8. Hybrid topology as inverter with active load: a) Equivalent circuit, b) Phasor diagram for feeding mode, c) Phasor diagram for regenerative mode.

IV. RESULTS

The first phase of the work was to evaluate the proposed topology and control method. Experimental results are included to show the controlled DC-link voltage of the H-Bridges and the current waveform improvement for the Hybrid Inverter. A second stage with simulation results showing the proposed converter operating as AFE rectifier,

using Matlab/Simulink coupled with the circuit simulator PSIM are also included.

The physical ratings of the considered converter are those of a 1kW laboratory prototype with a total DC-link voltage of Vdc = 180V and rated current of 10A. The capacitors used for the H-bridges are CH = 2200µF and their reference voltages have been set to V*H = 30V.

The control platform for this t of a DSP board with a Texas Instrument TMS320C6713 processor coupled with a daughter board based on a Xilinx/Spartan III FPGA including multiple A/D converters. In this configuration, the FPGA operates as a sampling clock, triggering the A/D conversions and interrupting the DSP. The processor is used for the calculation of all the controllers which results in a voltage reference for the converter, with this voltage reference the processor addresses the SHE tables and passes the information of commutation angles (αx and voltage phase to the FPGA. The FPGA performs the SHE modulation, the calculation of the harmonic references for the H-bridges and its unipolar PWM modulation using carrier frequency 2KHz.

A. Results for the inverter configuration

Experimental results are gained feeding a linear load with values RL = 10Ω and LL = 3mH with the 1kW prototype. As previously discussed in section III-C, the converter is operated with Vdc = 180V , while the H-Bridge dc-link voltage reference was set to 30V.

For comparison purposes, Fig. 9 shows the results for the NPC inverter operating without H-bridge compensation. In this result the NPC inverter is modulated by a 5-angle SHE pattern and m = 0.8. The first waveform corresponds to the NPC inverter output phase voltage va/ N which results in the 9-level load voltage waveform van of Fig.9b. Finally, Fig.9c shows the resulting output current waveform with its characteristic low frequency distortion.

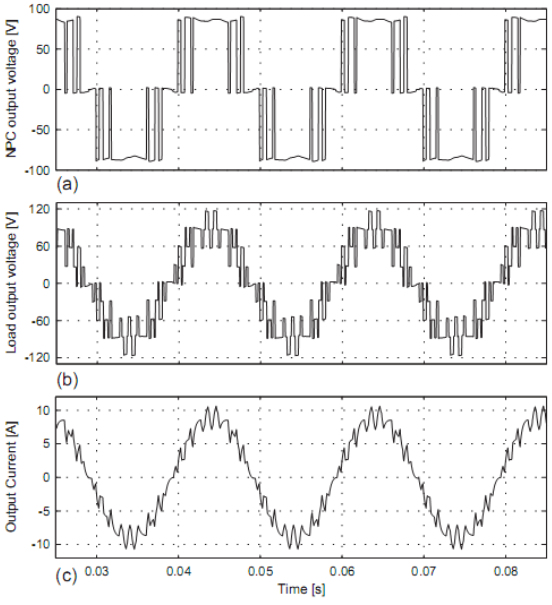

Fig. 9. NPC inverter operation at 50Hz with $m = 0.8$.

In comparison to the previous results, the full hybrid topol- ogy results are shown in Fig. 10. Fig. 10a shows the three- level NPC output voltage, va/ N , generated under the same conditions, while Fig. 10b shows the output voltage of the respective H-Bridge vaa/ . Note the higher switching frequency compared with the NPC output. Additional distortion can be

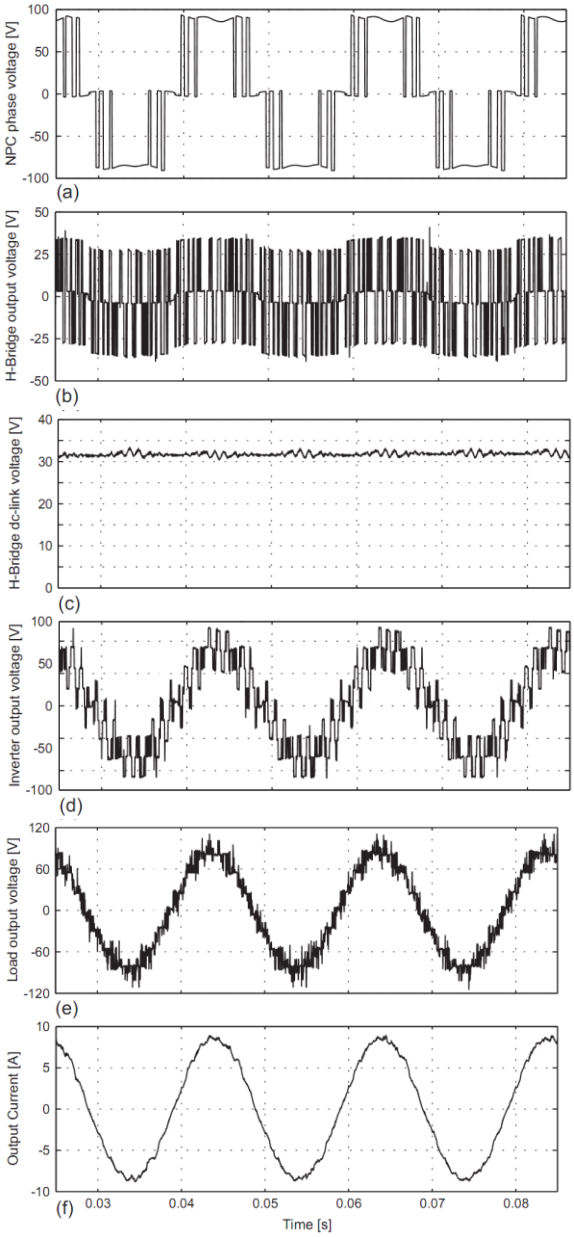

Fig. 10. Hybrid inverter operation at 50Hz with $m = 0.8$.

appreciated due to the semiconductors drop, which will not be relevant for higher voltage applications. The H-Bridge DC- link voltage is shown in Fig. 10*c*, which is controlled to be the desired voltage of $V_H = 0.167 \cdot V_{dc}$ as described in II-C. Also, it can be noted that in Fig. 10*e* that 33 different voltage levels are applied to the load voltage, causing less distortion in the output inverter waveforms than in the waveforms of Fig. 9. This is seen clearly in the current waveform in Fig. 10***f***, with a highly sinusoidal shape compared with the output current waveform without the H-Bridges harmonic compensation in Fig. 9*c*.

Hence, comparing the results of Fig. 9 with those of Fig. 10, it is clear that current waveform improvement has been achieved with the hybrid inverter. This is confirmed by the spectral analysis shown in Fig. 11. Here, the spectral content of simulated results corresponding to the steady state currents shown in Fig. 9*c* and 10***f*** are compared. For this analysis, simulated data is used to overcome inaccuracies, caused by use of a low voltage prototype, in particularly the effect of semiconductor drop. For the NPC converter, as expected, the spectrogram does not show the lower order harmonics. How- ever it does have more than 7% of the 17th and 19th harmonics and significant amplitude in higher order harmonics, resulting in a current THD of 12.9%. On the other hand, the operation of the hybrid converter shows almost a complete elimination of these characteristic harmonics, resulting in a current THD of 2.4%.

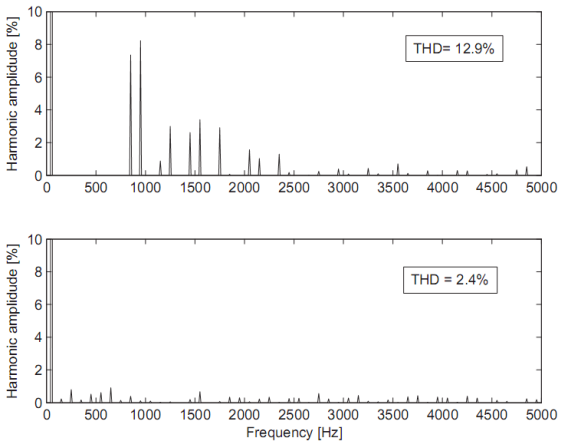

Fig. 11. Current spectrum for 50Hz operation with $m = 0.8$ a) NPC modulated by SHE. b) Full hybrid converter.

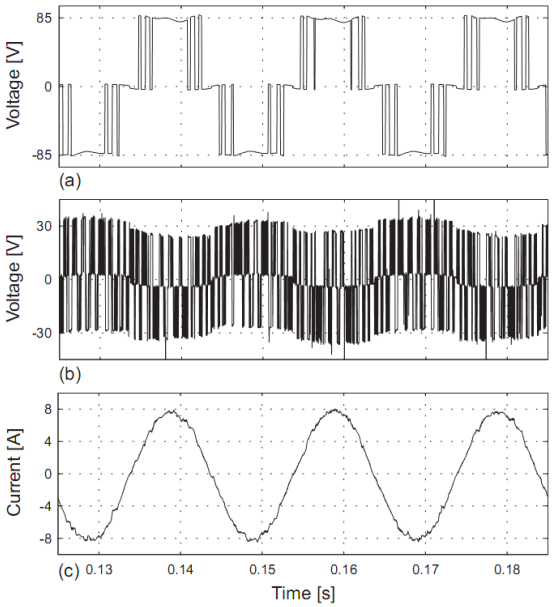

Fig. 12. Hybrid inverter 50Hz closed loop operation with Bandwidth of 160Hz, near $m = 0.81$: a) NPC voltage output of phase A; b) Voltage output of the H-Bridge A; c) Controlled load current.

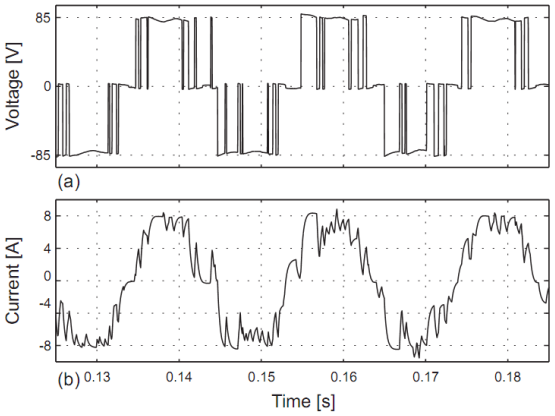

Fig. 13. NPC inverter 50Hz closed loop operation with Bandwidth of 160Hz, near $m = 0.81$: a) the NPC voltage output of phase A; b) Resulting load current.

B. Experimental results for current closed loop operation

This section presents results to ascertain converter's performance under closed loop conditions. First, the converter is run without the use of the series H-bridges (for comparison purposes only), and the results are shown in Fig. 13. It can be clearly seen that the output voltage of the converter in Fig. 13a suffers greatly due to the dynamic changes in modulation depth demanded by the output of the current control, hence constantly changing between patterns. This changing reference is produced by the feedback of the switching current harmonics that are significant in magnitude and can not be filtered by synchronous sampling. The resulting, heavily distorted, load current waveform is shown in Fig. 13b. This poor result is to be expected when linear current control is used with synchronous pulse patterns for the reasons given in III-B. In comparison, the results presented in Fig. 12 show highly sinusoidal current waveforms. The series H-bridges have compensated for the output distortion and enabled the use of a highly dynamic closed loop current control, without introducing additional commutation in the NPC bridge. The main objective of current waveform improvement has been achieved, thanks to the additional voltage levels introduced by the series connected H-Bridges, without the need for extra DC-link power supplies.

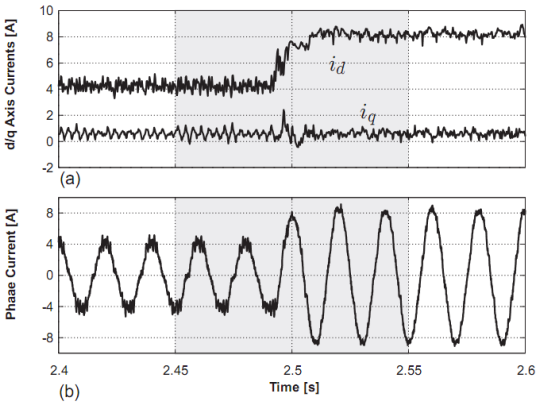

Fig. 14. Closed loop current response: a) Measured currents in the synchronous frame d/q; b) Phase current.

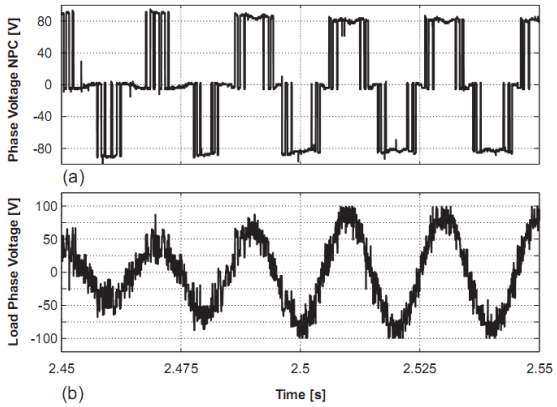

Fig. 15. Voltage during current step: a) NPC voltage response; b) Total load phase voltage.

The current loop dynamic response is shown in Fig. 14 and 15, where a step from 4A to 8A in the daxis current is commanded while the q axis current reference is kept constant. Note that no significant oscillations are present in the NPC voltage (as shown in Fig. 15a), which keeps operating with the 5-angle pattern, even during the current transient. During the transient however, small oscillations are present in the currents due to the limited compensation capability of the H-bridges, which is a result of their low voltage and to the limited amount of energy stored on them. Nevertheless, this additional oscillation decreases rapidly once the NPC stabilizes and reaches a quasi steady state.

C. Results for the active rectifier configuration

Figure 16 presents simulation results for the hybrid topology and control method when it is used as an active rectifier connecting a 115V line-to-line grid through a line impedance of Ls = 1.5mH and Rs = 0.2Ω. Note that at t = 0.14s, a change from feed to regenerative load mode has been demanded. This results in the change in polarity of the input current ia and in the NPC-SHE voltage output va/ N . The phase to neutral supply voltage van clearly shows the multilevel stepped waveform introduced by the NPC rectifier and the H-bridge series filter, which results in a high quality input current. The proposed DC-link control method exhibits good performance which can be observed in that the H-bridge DC- link voltage VH a remains close to the demanded Vdc /6, even though there is a change in the direction of power flow.

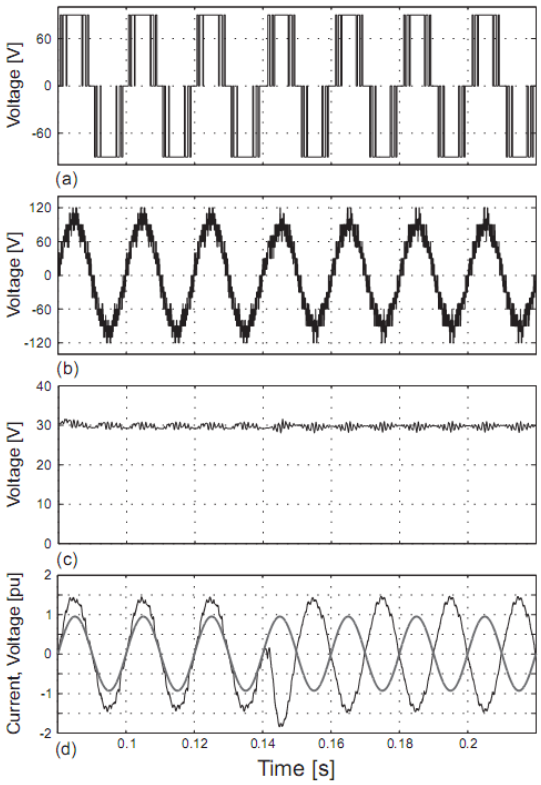

Fig. 16. Change from feeding to regenerating mode (at $t = 0.14$s) for the Hybrid Inverter: a) NPC-AFE phase voltage $v_{A'N}$; b) Line to neutral supply voltage v_{An}; c) H-bridge dc-link voltage V_{Ha}; d) Load current i_A of phase a in [pu] with 10A rated base and Active load voltage v_{sA} in [pu] with 100V rated base.

V. CONCLUSION

This paper presents the series connection of a SHE-modulated NPC and H-bridge multilevel inverter with a novel control scheme to control the floating voltage source of the H-bridge stage. The addition of the H-bridge series active filter or additional converter stage is not intended to increase the power rating of the overall converter. Rather, the main goal is to improve, in a controllable or active way, the power quality of the NPC bridge which may have a relatively low switching frequency. This enables superior closed loop performance for medium-voltage NPC-SHE based schemes, where this modulation strategy has been selected for efficiency purposes. It also allows the use of smaller inductive filters when connecting to the utility supply in AFE applications.

Since no changes are made to the power circuit and modulation stage of the NPC inverter, the series H-bridge power circuit and its control scheme can be easily added as an upgrade to existing NPC driven applications.

The proposed series H-bridge filter control scheme can be used either as a grid or load interface, depending on whether the NPC converter is used as an AFE or inverter respectively. Both possibilities can be combined if used in a back to back configuration.

The proposed floating dc-link voltage control scheme can be adapted to other hybrid topologies or cascaded H-bridge converters with the advantage that isolated input transformers can be avoided.

REFERENCES

[1] J. Rodr´ıguez, S. Bernet, B. Wu, J. Pontt and S. Kouro, "Multi- level voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec.2007.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodr´ıguez, M. Pe´rez and J. Leo´ n,"Recent Advances and Industrial Applications of Multilevel Converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] J.S. Lai and F.Z. Peng, "Multilevel converters-A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, no. 2, pp. 509–517, May/Jun. 1996.

[4] T. Meynard and H. Foch, "Multi-level choppers for high voltage appli- cations," Eur. Power Electron. J., vol. 2, no. 1, pp. 45–50, Mar. 1992.

[5] T. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob and M. Nahrstaedt, "Multicell converters: Basic concepts and industry ap- plications," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 955–964, Oct.

2002.

[6] M. Marchesoni, M. Mazzucchelli and S. Tenconi, "A non conventional power converter for plasma stabilization," IEEE Trans. Power Electron., vol. 5, no. 2, pp. 212–219, Apr. 1990.

[7] P. Hammond, "A new approach to enhance power quality for medium voltage AC drives," IEEE Trans. Ind. Appl., vol. 33, pp. 202–208, Jan./Feb. 1997.

[8] J. Rodr´ıguez, J. Pontt, G. Alzamora, N. Becker, O. Einenkel and A. Weinstein, "Novel 20 mw downhill conveyor system using three-level converters," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1093–1100, Oct. 2002.

[9] A. Yazdani and R. Iravani, "A neutral point clamped converter system for direct drive in variable speed wind power unit," IEEE Trans. Energy Conversion, vol. 21, pp. 596–607, Jun. 2006.

[10] J. Pou, R. Pindado and D. Boroyevich,"Voltage-balance limits in four- level diode-clamped converters with passive front ends," IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 190–196, Feb. 2005.

[11] G. Sinha and T. Lipo, "A four-level inverter based drive with a passive front end," IEEE Trans. Power Electron., vol. 15, no. 2, pp. 285–294, Mar. 2000.

[12] S. Busquets-Monge, S. Alepuz, J. Rocabert and J. Bordonau, "Pulsewidth modulations for the comprehensive capacitor voltage bal- ance of N-level three-leg diode-clamped converters," IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1364–1375, May 2009.

[13] N. Hatti, Y. Kondo and H. Akagi, "Five-level diode-clamped pwm converters connected back-to-back for motor drives," IEEE Trans. Ind. Appl., vol. 44, no. 4, pp. 1268–1276, Jul.-Aug. 2008.

[14] C. Rech and J. R. Pinheiro, "Impact of hybrid multilevel modulation strategies on input and output harmonic performances," IEEE Trans. Power Electron., vol. 22, pp. 967–977, May 2007.

[15] M. D. Manjrekar, P. K. Steimer and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," IEEE Trans. Ind. Appl., vol. 36, no. 3, pp. 834–841, May/Jun. 2000.

[16] S. Song, F. Kang and S.-J. Park, "Cascaded Multilevel Inverter Employ- ing Three-Phase Transformers and Single DC Input," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2005–2014, Jun. 2009.

[17] F. Z. Peng, J.-S. Lai, J. W. McKeever and J. Van Coevering, "A multilevel voltage-source inverter with separate DC sources for static VAr generation," IEEE Trans. Ind. Appl., vol. 32, no. 5, pp. 1130–1138, Sept./Oct. 1996.

[18] Q. Song, W. Liu and Z. Yuan, "Multilevel optimal modulation and dynamic control strategies for STATCOMs using cascaded multilevel inverters," IEEE Trans. Power Delivery, vol. 22, no. 3, pp. 1937–1946, Jul. 2007.

[19] G.-J. Su, "Multilevel DC-Link Inverter," IEEE Trans. Ind. Appl., vol. 41, no. 3, pp. 848–854, May/Jun. 2005.

[20] P. Lezana and J. Rodr´ıguez, "Mixed Multicell Cascaded Multilevel Inverter," in Proc. IEEE ISIE, 2007, pp. 509–514.

[21] D. Ruiz, R. Ramos, S. Mussa and M. Heldwein, "Symmetrical Hybrid Multilevel DC-AC Converters With Reduced Number of Insulated DC Supplies," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2307–2314, Jul. 2010.

[22] F. Kieferndorf, M. Basler, L. A. Serpa, J.-H. Fabian, A. Coccia and
G. A. Scheuer, "A new medium voltage drive system based on ANPC-5L technology," in Proc. IEEE-ICIT, 2010, pp. 605–611.

[23] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," IEEE Trans. Ind. Appl., vol. 41, no. 2, pp. 655–664, Mar./Apr. 2005.

[24] P. Steimer and M. Manjrekar, "Practical medium voltage converter topologies for high power applications," in Conf. Rec. IEEE IAS Annu. Meeting, 2001, pp. 1723 – 1730.

[25] T. Gopalarathnam, M. Manjrekar and P. Steimer, "Investigations on a unified controller for a practical hybrid multilevel power converter," in Proc. IEEE APEC, 2002, pp. 1024 –1030.

[26] C. Silva, P. Kouro, J. Soto and P. Lezana, "Control of an hybrid multilevel inverter for current waveform improvement" in Proc. IEEE ISIE, 2008, pp. 2329–2335.

[27] S. Bernet, R. Teichmann, A. Zuckerberger and P. Steimer, "Comparison of high-power igbt's and hard-driven gto's for high-power inverters," IEEE Trans. Ind. Appl., vol. 35, no. 2, pp. 487–495, Mar./Apr. 1999.

[28] J. Holtz and N. Oikonomou, "Estimation of the fundamental current in low-switching-frequency high dynamic medium-voltage drives," IEEE Trans. Ind. Appl., vol. 44, no. 5, pp. 1597–1605, Sept./Oct. 2008.

[29] B. Wu, High-Power Converters and AC Drives. Wiley-IEEE Press, 2006. [30] L. Cordova, C. Silva and P. Lezana, "Hybrid multilevel inverter drive with synchronous modulation and current waveform improvement," in

Proc. IEEE IEMDC, 2009, pp: 158-164.

[31] C. Rech and J. R. Pinheiro, "Hybrid multilevel converters: Unified analysis and design considerations," IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 1092–1104, Apr. 2007.

[32] Technical Information – IGBT Module FZ1200R17HP4, Infinion, http://www.infinion.com/, 2010.

[33] Data Sheet – Reverse Conducting IGCT 5SHX 14H4510, ABB Semiconductors, www.abb.com/semiconductors, Lenzburg, Switzerland,

2007.

[34] T. Salzmann, G. Kratz and C. Daubler, "High-power drive system with advanced power circuitry and improved digital control," IEEE Trans. on Ind. Appl., vol. 29 , no. 1, pp. 168–174, Jan./Feb. 1993.

[35] J. Holtz and N. Oikonomou, "Synchronous optimal pulsewidth modula- tion and stator flux trajectory control for medium-voltage drives," IEEE Trans. Ind. Appl., vol. 43, no. 2, pp. 600–608, Mar./Apr. 2007.

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